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DETAILED ACTION

Drawings

Figures 1(a), 1(b), 2(a) and 2(b) should be designated by a legend such as --Prior Art--because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Allowable Subject Matter

Claims 1-18 are allowable over the prior art of record.

The following is an examiner's statement of reasons for allowance: Although Kwon (US PAT No. 6,316,962) teaches a reversible adiabatic logic circuit, one of ordinary skill in the art would not have been motivated to modify the teaching of Kwon to further includes, among other things, the specific of state determination means whether the reversible logic element is in the A-state or the B-state where if the state determinations means determines that the reversible logic element is in the A-state and the signal is input from the input line T, then the state determination means conveys information that the reversible logic element is in the A-state to the control means, the input information identification means conveys the information that the signal is input from the input line T to the control means, and the control means controls the output

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means to output the signal to the output line T_A and controls the state control means to change the state of the reversible logic element to the B-state as set for the claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Frank (US PAT No. 5,493,240) discloses static combinational logic circuits for reversible computation.

Miller (Spectral and Two-Place Decomposition Techniques in Reversible Logic, 2002 IEEE) discloses reversible logic gates using Rademacher-Walsh spectral techniques and two-place decomposition of Boolean functions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Cho whose telephone number is 571-272-1802. The examiner can normally be reached on M-F 6:30 AM - 3:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

James H. Cho Primary Examiner Art Unit 2819

July 8, 2005